Attorney Docket No.: 15057US02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the Application of:

Kimming So, et al.

Serial No.: 10/750,523

Filed: December 31, 2003

For: A MINI-TRANSLATION LOOKASIDE BUFFER FOR USE IN MEMORY TRANSLATION

Examiner: Yaima Campos

Group Art Unit: 2185

Conf. No.: 1971

Electronically Filed on December 15, 2008

REPLY BRIEF

Board of Patent Appeals and Interferences
U.S. Patent and Trademark Office
PO Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with 37 CFR 41.41, Appellants submit this Reply Brief in response to the Examiner's Answer mailed on October 15, 2008.

STATUS OF THE CLAIMS

The present Application originally included Claims 1-20. Claims 1-11 have been cancelled and Claims 21-44 have been added. Pending Claims 12-44 stand rejected and are the subject of the appeal.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 12-23, 25, 29-34, and 41-43 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Hinton et al. (U.S. Patent No. 5,500,948) (hereinafter, Hinton). Claim 24 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Hinton. Claims 26 and 44 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hinton in view of Bryg et al. (U.S. Patent No. 6,430,670) (hereinafter, Bryg). Claims 27-28 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hinton in view of Riedlinger et al. (U.S. Patent No. 6,446,187) (hereinafter, Riedlinger). Claims 35-38 and 40 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicant Admitted Prior Art (hereinafter, AAPA) in view of Hinton. Claim 39 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over AAPA in view of Hinton as applied to Claim 38 above, and further in view of Bryg.

ARGUMENT

GENERAL COMMENTS

The Appellants maintain the arguments presented in the Appeal Brief dated July 30, 2008. The Appellants have responded to the Examiner's Answer starting from section (10) (i.e., Response to Argument), since section (9) (i.e., Grounds of Rejection) restates what was previously presented in the Office Action dated October 29, 2007.

RESPONSE TO ADVISORY ACTION

In the Examiner's Answer, the Examiner stated the following:

> Appellant has provided arguments in response to Advisory Action mailed on January 8, 2008; however, these arguments parallel arguments presented regarding rejection of claims 12-44 and have been addressed in the same manner. See bellow. [sic]
>
> For the most part, Appellant appears to be reading limitations into the claims which are not being claimed; however, the claims have been interpreted according to the broadest reasonable interpretation available to one of ordinary skill in the art wherein limitations that are not recited in the claims have not been read into the claims (M.P.E.P. 2111 [R-1]).

See Examiner's Answer at pages 24-25.

Absent any specificity in her argument, the Appellants respectfully disagree with the Examiner's remark that the Appellants appear to be reading limitations into the claims. On the other hand, and contrary to what the Examiner alleges, the Appellants respectfully submit that

the Examiner has not shown a teaching of *what is recited* in the pending claims. Furthermore, in an attempt to show a teaching of the pending claims, the Appellants believe that the Examiner has provided improper interpretations of the subject matter recited in the pending claims as well as improper characterizations of the verbiage in the cited references.

I. REJECTION OF CLAIMS 12-23, 25, 29-34 AND 41-43 UNDER 35 U.S.C. § 102(b) BY HINTON

A. Independent Claim 12

In the Examiner's Answer, the Examiner stated the following:

> Appellant argues Hinton does not disclose "consolidating even and odd page frame numbers into a single page frame number field" as recited by claim 12 as Hinton utilizes two separate memories to store even and odd pages, as a consequence, the method disclosed by Hinton provides no reduction in memory size.'
>
> In response, this argument has been fully considered, but it is not deemed persuasive.
>
> First, the Examiner would like to respectfully point out that pending claim 12 has been interpreted according to the broadest reasonable interpretation wherein limitations requiring reduction in size or requiring the same or separate memories to define a single field are not recited in the rejected claim 12. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See In re Van Geuns, 988 F.2d 1181,26 USPQ2d 1057 (Fed. Cir. 1993).
>
> The limitation "a single field" (as claimed) has been interpreted according to the broadest reasonable interpretation wherein a field is known in the art as a location in which a particular type of data is stored (Refer to Microsoft Computer Dictionary, Fifth Edition). Note that in Hinton, the combination of registers 104 and 106 is used to store logical and physical address sets (which comprises a

> particular type of data); therefore, the combination of these registers has been interpreted as a single field in which logical to physical address sets or a particular data type is stored [Refer to Hinton (col. 6, lines 37-63; fig. 3 and related text)].

Claim 12 recites "a method of improving the performance of address translation in a translation lookaside buffer comprising: using a bit obtained from a virtual page number to indicate whether a page frame number is even or odd; and consolidating even and odd page frame number fields into a single page frame number field of said translation lookaside buffer."

The Appellants disagree that the Claim 12 has been interpreted according to the broadest reasonable interpretation, as alleged by the Examiner. Appellants feel that the Examiner has improperly characterized what is disclosed in the cited references and in Claim 12 in an attempt to show a teaching of Claim 12. For example, it is apparent that the Examiner has not accurately stated what is actually recited in Claim 12. Claim 12 does not recite "a single field" as alleged by the Examiner. Instead, Claim 12 recites "a single page frame number field" of a translation lookaside buffer. Thus, for at least this reason, the Examiner has not shown a teaching of Claim 12. Furthermore, the Examiner has improperly characterized the definition of the term "field" provided by the Microsoft Computer Dictionary, Fifth Edition. Citing the Microsoft Computer Dictionary, Fifth Edition, the Examiner has defined the term, field, as "a location in which a particular type of data is stored." In comparison, the Appellants respectfully submit that the Microsoft Computer Dictionary, Fifth Edition, actually states that the term, field, is defined as "a location *in a record* in which a particular type of data is stored."

Microsoft Computer Dictionary, Fifth Edition, defines field as follows:

> 1. A location in a record in which a particular type of data is stored. For

> example, EMPLOYEE-RECORD might contain fields to store Last-Name, First-Name, Address, City, State, Zip-Code, Hire-Date. Current-Salary. Title, Department, and so on. Individual fields are characterized by their maximum length and the type of data (for example, alphabetic, numeric, or financial) that can be placed in them. The facility for creating these specifications usually is contained in the data definition language (DDL). In relational database management systems, fields are called columns.

Therefore, the Examiner has improperly characterized what is disclosed in the Microsoft Computer Dictionary, Fifth Edition. Thus, based on this improper characterization, the Examiner does not show a teaching of Claim 12.

The Examiner further alleges that "a field is known in the art as a location in which a particular type of data is stored." Based on the definition provided by Microsoft Computer Dictionary, Fifth Edition, there is no indication that "a field is known in the art as a location in which a particular type of data is stored," as the Examiner alleges. While Microsoft Computer Dictionary, Fifth Edition, discloses that a field is defined as a location in a record, in which, for example, an employee record is created by way of data definition language associated in a relational database, nowhere does Microsoft Computer Dictionary, Fifth Edition, state anything about "a field (is known in the art) as a location in which a particular type of data is stored." Consequently, the Examiner's reasoning does not lend itself to showing a teaching of Claim 12.

The Examiner alleges that "the combination of registers 104 and 106 is used to store logical and physical address sets or [sic] a particular data type is stored." Furthermore, the Examiner alleges that "therefore, the combination of these registers has been interpreted as a single field in which logical to physical address sets or a particular data type is stored." Based on the foregoing, the Examiner has attempted to show a teaching of Claim 12 by way of using

multiple improper characterizations of the cited reference and the subject matter in Claim 12. For example, the Examiner attempts to show a teaching of a *single field* (which does not teach "a single page frame number field") using Hinton's *combination of registers* (Examiner's concept of *location* as opposed to *location in a record, in which the Examiner interprets location as a combination of registers*). Since the Appellants respectfully submit that the Examiner arrives at these conclusions through multiple improper characterizations, the Examiner has not shown a teaching of what is recited in Claim 12. Therefore, based on the foregoing reasons, the Appellants respectfully request reversal of the rejection.

Furthermore, even if the Examiner had not improperly characterized the cited reference or Claim 12, the Appellants respectfully submit that the Examiner would not have shown a teaching of "using a bit obtained from a virtual page number to indicate whether a page frame number is even or odd; and consolidating even and odd page frame number fields into a single page frame number field of said translation lookaside buffer," as recited in Claim 12. For example, the Examiner's reference to Hinton, at col. 6, lines 37-63, may disclose using even and odd registers within a translation write buffer (as specified in Hinton, at Figure 3); however, there is no disclosure within Hinton of "using a bit obtained from a virtual page number to indicate whether a page frame number is even or odd; and consolidating even and odd page frame number fields into a single page frame number field of said translation lookaside buffer," as recited in Claim 12.

Referring to Figure 3, Hinton describes the registers in his TWB (translation write buffer), at col. 6, lines 56-59, as follows:

> Registers (106) marked "0" are for even-numbered 4KB pages, addresses

> for which bit 12 is a zero. Registers ((104) marked "1" are for odd-numbered 4KB pages, addresses for which bit 12 is a one.

Thus, Hinton, at col. 6, lines 56-59, indicates nothing about how a pair of registers could be interpreted as a single field. Furthermore, one of ordinary skill in the art would know that a register does not teach a field of a record. In addition, Hinton teaches away from what is recited in Claim 12, since Hinton describes using separate registers for odd numbered pages and even numbered pages. As a consequence, Hinton could not possibly disclose any consolidation of even and odd page frame number fields. Thus, based on the foregoing, the Examiner has not shown a teaching of "consolidating even and odd page frame number fields into a single page frame number field of said translation lookaside buffer," as recited in Claim 12. Consequently, based on the foregoing, the Appellants respectfully request a reversal of the rejection to Claim 12.

On pages 26-27, the Examiner recites paragraph 26 of Appellants' specification, which states the following:

> The Examiner would also like to point out that Appellant's Specification describes storing even and odd page frame numbers into a single page frame number field of said translation lookaside buffer as ["Figure 3 is a relational block diagram illustrating an organizational structure of a mini-TLB system 300 in accordance with an embodiment of the invention. The mini-TLB system 300 comprises a miniature version of the previously mentioned translation lookaside buffer described in Figure 1 (herein termed a mini-TLB 304) communicating with a number of mini-TLB registers 308 and a control processor 324. In one embodiment, the mini-TLB 304 is configured by way of instructions executed by the control processor 324. For the mini-TLB 304 shown in Figure 3, the index and

page mask registers function in the same manner as was described earlier in Figure 1. In addition, virtual addressing is performed using the addressing format described in Figure 2, in which a 32 bit virtual address is used. Of course, it is contemplated that in other embodiments, virtual addressing may be performed using more or less than 32 bits. In the embodiment shown, the entry Hi 312 register of Figure 3 facilitates storage and read out of a virtual page number associated with bits [31:12] of the virtual addressing format discussed previously. Hence, as illustrated in Figure 3, the virtual page number (VPN) may be either read from or written into a VPN field (or section) 316 of the mini-TLB 304. The VPN is associated with a page frame number (PFN) which is similarly either read from or written into a PFN field 320 of the mini-TLB 304 using the registers shown (i.e., entry Lo0 or entry Lo1 registers). In the embodiment illustrated in Figure 3, only one of the entry Lo registers (either entry Lo0 or entry Lon is valid for use during a write operation; for example, the contents of a valid entry Lo register is written into the page frame number (PFN) field 320 associated with a specified page table entry of the mini-TLB 304. In one embodiment, the least significant bit (lsb) of a VPN (i.e., bit 12 of the 32 bit virtual address described) is used to determine whether the entry Lo0 or an entry Lo1 register contains valid data for writing into the PFN field 320 of the mini-TLB 304. Similar principles may be applied during a read from the mini-TLB 304. For example, the least significant bit (lsb) of the VPN may be used to determine which register, either entry Lo0 or entry Lo1, will be used to access valid page frame number data utilized by the control processor 324 during a read operation. In a read operation, for example, the least significant bit (lsb) of a virtual page number is used to store data into either the entry Lo0 register or the entry Lo1 register. In this fashion, both even and odd page frame numbers may be stored or recalled from a single page frame number field of the mini-TLB 304" (Appellant's Specification, Paragraph 0026)]. Therefore, Appellant's Specification discloses two registers and reading/writing to only one of these two registers when reading/writing to TLB. Emphasis added on underlined portions.

Based on Appellants' specification, the Examiner alleges that "Appellants' specification discloses two registers and reading/writing to only one of these two registers when reading/writing to TLB." Contrary to what the Examiner alleges, paragraph 26 of the specification does not disclose "two registers and reading/writing to only one of these two registers when reading/writing to TLB." Instead, paragraph 26 of the specification discloses two registers for reading/writing to a one page frame number (PFN) field 320 of the mini-TLB 304. Consequently, the Examiner has further mischaracterized what is actually presented in paragraph 26 of the Appellants' specification in an attempt to show a teaching of Claim 12. Thus, the Examiner has not shown a teaching of Claim 12. For at least this reason, the Appellants request reversal of this rejection.

The Examiner goes on to state the following at pages 27-28 of the Examiner's Answer:

> In light of the foregoing, Hinton discloses "consolidating even and odd page frame numbers into a single page frame number field" as according to Hinton's disclosure; [when bit 12 is a 0, TWB (Translation Write Buffer or mini-TLB) will read and write in a single field within Physical Register 0 (which is used for even pages), which comprises reading and writing even page frame numbers into a single page frame number field of a translation lookaside buffer. For further explanation, when bit 12 is a 1, TWB will read and write into a single field within Physical Register 1 (which is used for odd pages), which comprises consolidating even and odd page frame numbers into a single page frame number field]. Note that registers 104 (odd pages) and 106 (even pages) used to store even and odd logical to physical address sets are interpreted as a single page frame number field for even and odd page frame numbers; even page frame number are

only stored in register 106 and odd page frame numbers are only stored in register 104. Therefore, Hinton discloses, "consolidating even and odd page frame numbers into a single page frame number field" of a translation lookaside buffer, as claimed by Appellant. Refer to the following in Hinton's disclosure ["Mini-TLB (TWB)," defined as "A small 3-entry instruction mini TLB (6)" (Columns 5-6, lines 62-67 and 1-5) to provide access to memory wherein "the instruction pointer is comprised of logical address bits including upper order bits, lower order bits, and a single bit having a first value or a second value, the single bit providing for translation of even-number pages for which the single bit has a first value and for odd-number pages for which the single bit has the second value" (Columns 1-2, lines 64-67 and 1-29; Column 6, lines 37-63; Figure 3) "TWB" (mini TLB) (Figure 3, Diagram of TWB) in which "a logical address (81) is separated into three parts... Bit 12 selects which of the two entries in the TWB are to be used for this address... Registers (106) marked "0" are for even-numbered 4KB pages, addresses for which bit 12 is a zero. Registers (104) marked "1" are for odd-numbered 4KB pages, addresses for which bit 12 is a one" (Column 6, lines 37-63) wherein for a TWB load, "one set (even or odd) of the TWB registers in loaded with the logical and physical addresses" (Column 7, lines 5-14)].

The Examiner's argument on pages 27-28 of the Examiner's Answer does not show a teaching of Claim 12 since it is based on the improper characterizations previously explained by the Appellants. For example, the Examiner assumes that "that registers 104 (odd pages) and 106 (even pages) used to store even and odd logical to physical address sets are interpreted as a single page frame number field for even and odd page frame numbers." As the Appellants had previously argued, the combination of registers 104, 106 does not teach a single page frame number field. Instead, Hinton discloses an implementation of a translation write buffer (TWB) using separate registers, for even (106) and odd (104) pages, respectively, as may be clearly seen in Figure 3 of Hinton.

The Appellants respectfully request the Board to refer to Hinton, at col. 6, lines 56-59, which states that:

> Registers (106) marked "0" are for even-numbered 4KB pages, addresses for which bit 12 is a zero. Registers ((104) marked "1" are for odd-numbered 4KB pages, addresses for which bit 12 is a one.

Consequently, for at least the foregoing reasons, Hinton teaches away from what is recited in Claim 12. Hinton teaches away from "using a bit obtained from a virtual page number to indicate whether a page frame number is even or odd; and consolidating even and odd page frame number fields into a single page frame number field of said translation lookaside buffer," as recited in Claim 12. Hinton's teachings are different from "consolidating even and odd page frame number fields into a single page frame number field of said translation lookaside buffer," as recited in Claim 12. Furthermore, Hinton does not disclose anything about "consolidating even and odd page frame number fields into a single page frame number field of said translation lookaside buffer." Thus, for at least these reasons, the Appellants respectfully request reversal of the rejection to Claim 12.

The Examiner goes on to state the following at page 29 of the Examiner's Answer:

> Further, the Examine [sic] would like to emphasize, that contrary to Appellant's assertion, Hinton discloses reducing the size of the TLB, as a reduction in size is a generic property in Hinton's TWB wherein Hinton discloses ["Mini-TLB (TWB)," defined as "A small 3-entry instruction mini TLB (6)" (Columns 5-6, lines 62-67 and 1-5) which is of mini/reduced size (thus, a size reduction is a generic property of Hinton's TWB or mini-TLB). Appellant should note that by using "a single bit having a first value or a second value, the single bit providing for translation of even-number pages for which the single bit has a

> first value and for odd-number pages for which the single bit has the second value" (Columns 1-2, lines 64-67) wherein even-number pages will only be written within "physical register 0 - 106" and odd-number pages will only be written within "physical register 1 -104;" therefore, having a single entry for each page depending on the value of bit 12 and implementing a TLB of reduced size or mini-TLB, as claimed (See Figures 3 and 7 and related text)].

Contrary to what the Examiner alleges, the foregoing remarks made by the Examiner do not show a reduction in size of any buffer as a result of consolidating even and odd page frame number fields into a single page frame number field. The Examiner has not shown a teaching of "consolidating even and odd page frame number fields into a single page frame number field of said translation lookaside buffer," as recited in Claim 12. Further, the Examiner's statement that "Hinton discloses reducing the size of the TLB, as a reduction in size is a generic property in Hinton's TWB," is unsupported in Hinton, since Hinton actually teaches away from any reduction in size, as Hinton employs the use of separate even and odd registers to store even and odd page frame numbers, respectively. Thus, for at least these reasons, the Examiner has not shown a teaching of Claim 12. Therefore, the rejection should be reversed and Claim 12 should be advanced to allowance.

The Examiner goes on to state the following at pages 29-31 of the Examiner's Answer:

> Appellant remarks that Hinton does not teach a page frame number field as an even or odd logical and physical address set is not a page frame number field.
>
> In response, this remark has been fully considered, but it is not deemed persuasive.
>
> A page frame comprises a physical address to which a page of

virtual/logical memory may be mapped (according to Microsoft Computer Dictionary, Fifth Edition), wherein virtual/logical to physical address mappings use page frame number to map virtual/logical pages to physical frames; thus, translation sets of virtual/logical and physical addresses inherently comprises page frame numbers. Therefore, contrary to Appellant's remarks, Hinton discloses a page frame number (as claimed) as [Refer to logical address (col. 6, lines 37-44) "the instruction pointer is comprised of logical address bits" (Col. 2, lines 9-10) "TWB is loaded with the logical and physical addresses" (col. 7, lines 12-14 and 43-46) wherein "registers (106) marked "0" are for even-numbered pages, addresses for which bit 12 is a zero. Registers (104) marked "1" are for odd-numbered 4KB pages, addresses for which bit 12 is a one" (Column 6, lines 37-63; Figure 3)].

Appellant argues Hinton's translation write buffer (TWB) does not teach a translation lookaside buffer (TLB) as Hinton's TWB comprises elements that are functionally different from Appellant's claimed invention.

In response, this argument has been fully considered, but it is not deemed persuasive since features referring to the alleged functional differences are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See In re Van Geuns, 988 F.2d 1181,26 USPQ2d 1057 (Fed. Cir. 1993); wherein the pending claims simply require a translation lookaside buffer, which Hinton clearly discloses as ["Mini-TLB (TWB)," defined as "A small 3-entry instruction mini TLB (6)" (Columns 5-6, lines 62-67 and 1-5)]; therefore, TWB comprises a TLB or translation lookaside buffer, as claimed.

Appellant argues the Examiner has failed to provide a logical explanation as to how Hinton may be used to show a teaching of claim 12 and that "for example, the Examiner has failed to show a teaching of "using a bit obtained from a virtual page number to indicate whether a page number is even or odd."

This argument has been fully considered; however, the Examiner strongly disagrees as Hinton discloses "using a bit obtained from a virtual page number to

> indicate whether a page number is even or odd" as ["A logical address (81) is separated into three parts. Bits 0 through 11 are an offset within an instruction page" and explains that "bit 12 selects which of the two entries in the TWB (62) are to be used for this address... registers (106) marked "0" are for even-numbered pages, addresses for which bit 12 is a zero. Registers (104) marked "1" are for odd-numbered 4KB pages, addresses for which bit 12 is a one" (Column 6, lines 37-63; Figure 3)].

Contrary to what the Examiner alleges, the Appellants respectfully submit that a page frame number field is not taught by an even or odd logical and/or physical address set. The Appellants respectfully wonder how a field is taught by an address set. Furthermore, the Examiner resorts to Microsoft Computing Dictionary, Fifth Edition, in order to obtain the definition of page frame. Microsoft Computing Dictionary, Fifth Edition defines page frame as follows:

> A physical address to which a page of virtual memory may be mapped.

Thus, based on the foregoing, it is evident that a physical address does not teach a page frame number field, as recited in Claim 12, since a field is different from an address or address set. Consequently, for at least this reason, the Examiner has not shown a teaching of what is recited in Claim 12. Therefore, the Appellants respectfully request reversal of the rejection to Claim 12.

The Examiner makes an attempt to show a teaching of "using a bit obtained from a virtual page number to indicate whether a page frame number is even or odd," as recited in Claim 12. In an attempt to show a teaching, the Examiner refers to Hinton, at col. 6, lines 37-63 and at Figure 3. However, Hinton, at col. 6, lines 37-63, discloses nothing more than logical

addresses (bits 13-31) addressing a first logical register 108 and a second logical register 110. The Appellants respectfully submit that Hinton, at col. 6, lines 37-63, does not disclose anything about "using a bit obtained from a virtual page number to indicate whether a page frame number is even or odd," as recited in Claim 12. For example, Hinton, at col. 6, lines 37-63, does not disclose anything about "using a bit obtained from a virtual page number." While Hinton may disclose using bit 12 to select between addressing one of two registers, Hinton does not disclose anything about "using a bit obtained from a virtual page number to indicate whether a page frame number is even or odd," as recited in Claim 12. Thus, for at least these reasons, the Examiner has not shown a teaching of Claim 12.

Thus, based on each of the foregoing reasons, the Appellants request a reversal of the rejection to Claim 12. Appellants believe that Claim 12 contains patentable subject matter that should be advanced to allowance.

B. Dependent Claim 15

In the Examiner's Answer, the Examiner states the following:

> Appellant's arguments directed to the rejection of claim 15, for the most part, reiterate the alleged deficiencies Appellant pointed out with respect to independent claim 12. Accordingly, these arguments are addressed at least in the manner that claim 12 has been addressed above.
>
> Claim 15, however, recites the previously argued (and not recited in claim 12) limitation of "consolidating... implements a translation lookaside buffer of reduced size;" wherein Appellant argues Hinton does not disclose this limitation. However, as pointed out above, this argument is not deemed persuasive as a reduction in size is a generic property in Hinton's TWB wherein Hinton discloses ["Mini-TLB (TWB)," defined as "A small 3-entry instruction mini TLB (6)"

> (Columns 5-6, lines 62-67 and 1-5) which is of mini/reduced size. Appellant should note that by using "a single bit having a first value or a second value, the single bit providing for translation of even-number pages for which the single bit has a first value and for odd-number pages for which the single bit has the second value" (Columns 1-2, lines 64-67) wherein even-number pages will only be written within "physical register 0-106" and odd-number pages will only be written within "physical register 1-104;" therefore, having a single entry for each page depending on the value of bit 12 and implementing a TLB of reduced size or mini-TLB (as expressly named by Hinton), as claimed (See Figures 3 and 7 and related text)].
>
> *See* Examiner's Answer at pages 31-32.

Claim 15 recites "the method of Claim 12 wherein said consolidating even and odd page frame number fields into said single page frame number field implements a translation lookaside buffer of reduced size." Contrary to what the Examiner alleges, the Appellants respectfully argued that Claim 12 contains patentable subject matter, as the Appellants respectfully pointed out the deficiencies with respect to the Examiner's arguments. Appellants believe that Claim 15 is in condition for allowance for the reasons pointed out in Appellants' argument for Claim 12. Since the Examiner alleges that she has addressed Claim 15 in the same manner as she did for Claim 12, the Appellants request the Board to consider Appellants' arguments for Claim 12. As was stated in Appellants' argument for Claim 12, the Examiner's statement that "Hinton discloses reducing the size of the TLB, as a reduction in size is a generic property in Hinton's TWB," is unsupported in Hinton, since Hinton actually teaches away from any reduction in size, as Hinton employs the use of separate even and odd registers to store even and odd page frame numbers, respectively. Therefore, for at least this reason, Claim 15 contains patentable subject matter that should be passed to allowance.

Furthermore, Hinton, at cols. 5-6, lines 62-67 and 1-5, does not teach anything about "wherein said consolidating even and odd page frame number fields into said single page frame number field implements a translation lookaside buffer of reduced size," as recited in Claim 15. Hinton, at cols. 5-6, lines 62-67 and 1-5, states:

> A small 3-entry instruction mini TLB (62) named a translation write buffer (TWB) is provided. Two of the three entries are used for normal instruction-fetch logical-tophysical address translations. These two entries are accessed in a "direct-mapped" manner. This uses bit 12 from the IP to select which of the two entries to use for a particular IP translation. This is effectively a 2-1 multiplexor that can operate in a very short period of time to meet the speed requirements mentioned above for the early-fetch and splitline Instruction cache mechanisms. Because of good instruction "locality," this two entry TWB gets a good hit rate.

While Hinton, at cols. 5-6, lines 62-67 and 1-5, may disclose a buffer of reduced size, there is no disclosure in Hinton that provides support for a translation lookaside buffer of reduced size that is implemented by way of consolidating even and odd page frame number fields into said single page frame number field. In particular, Hinton, at cols. 5-6, lines 62-67 and 1-5, does not disclose anything about "consolidating even and odd page frame number fields into said single page frame number field." Therefore, for at least this reason, Claim 15 contains patentable subject matter that should be passed to allowance.

C. Independent Claim 16

In the Examiner's Answer, the Examiner states the following:

> Appellant's arguments directed to the rejection of claim 16, for the most

> part, reiterate the alleged deficiencies Appellant pointed out with respect to independent claim 12. Accordingly, these arguments are addressed at least in the manner that claim 12 has been addressed above.
>
> Appellant argues Hinton does not disclose "a buffer that uses a single page frame number field for storing odd/even page frame numbers" as required by claim 16; however, the Examiner strongly disagrees as Hinton discloses [TWB having a single field for storing odd page frame numbers and a single field for storing even page frame numbers (col. 6, lines 37-63; fig. 3 and related text); thus disclosing a single page frame number field for storing odd/even page frame numbers. Further note that registers 104 and 106 in Hinton are interpreted to correspond to a single field]. See response to [A. Independent claim 12] above. Further, the limitation "a buffer that uses a single page frame number field for storing odd/even page frame numbers" appearing in system claim 16, has been interpreted intended use, and as such the claim does not require the buffer actually perform the listed functionality of storing odd/even page frame numbers, but merely that the function not be expressly precluded. See MPEP 2106 II(C).
>
> *See* Examiner's Answer at page 33.

Claim 16 recites "a system to provide effective virtual to physical memory address translation comprising a buffer that uses a single page frame number field for storing odd/even page frame numbers." Contrary to what the Examiner alleges, the Appellants respectfully argued that Claim 12 contains patentable subject matter. Appellants believe that Claim 16 is in condition for allowance for at least the reasons pointed out in the previous section for Claim 12. Furthermore, the Appellants had pointed out the deficiencies with respect to the Examiner's arguments for Claim 12. Since the Examiner indicates that she wishes to address Claim 16 in the same manner as she did for Claim 12, the Appellants request the Board to consider Appellants' arguments for Claim 12. It appears that the Examiner has made the same argument she made in the Office Action dated October 29, 2007 in which the Appellants had already addressed in the

Appeal Brief dated July 30, 2008. Consequently, the Appellants maintain the arguments presented in the Appeal Brief.

Hinton, at col. 6, lines 37-63, states:

> FIG. 3 is a block diagram of the translation write buffer (TWB). A logical address (81) is separated into three parts. Bits 0 through 11 are an offset within an instruction page, and are passed through to the physical address unmodified. Bit 12 selects which of the two entries in the TWB (62) are to be used for this address. Bits 13 through 31 are compared against the stored logical address in the TWB. If these bits mismatch, it is considered a TWB miss, and the physical address from the TWB is considered invalid. If the bits match, it is considered a TWB hit, and the physical address bits 12 through 31 stored in the TWB are driven out to the cache on output cache physical address (83) and/or on output physical address (80) to the physical address bus. The logical registers (108, 110) compare the logical address (81) presented to the IFU with stored values. The hit 1 line indicates to the control logic (112) that a match occurred in logical register 1 (108). The hit 0 line indicates to the control logic (112) that a match occurred in logical register 0 (110). The physical registers (104, 106) provide stored-physical addresses to the MUX (100). Registers (106) marked "0" are for even-numbered 4KB pages, addresses for which bit 12 is a zero. Registers ((104) marked "1" are for odd-numbered 4KB pages, addresses for which bit 12 is a one. The microcode base register holds the microcode base address. The MUX (100) selects one of the three physical address registers and drives the physical address buses. The control logic block (112) coordinates the actions of the other blocks.

Based on the foregoing passage, Hinton, at col. 6, lines 37-63 and Fig. 3 of Hinton, discloses *two* distinct and separate registers for storing "physical addresses," which does not teach what is recited in Claim 16. Hinton, at col. 6, lines 54-59 states:

> The physical registers (104, 106) provide stored-physical addresses to the MUX (100). Registers (106) marked "0" are for even-numbered 4KB pages, addresses for which bit 12 is a zero. Registers ((104) marked "1" are for odd-numbered 4KB pages, addresses for which bit 12 is a one.

As may be easily seen from the above passage from Hinton, Hinton's physical register 104 is simply used to store odd numbered pages while Hinton's physical register 106 is simply used to store even numbered pages. Based on what is disclosed in Hinton, at col. 6, lines 54-59, there is no disclosure of "a buffer that uses a single page frame number field for storing odd/even page frame numbers," as recited in Claim 16. As the Appellants had demonstrated in Claim 12, the Examiner attempts to show a teaching of a *single field* (which does not teach "a single page frame number field") using Hinton's *combination of these registers* (Examiner's concept of *location* as opposed to *location in a record*), by way of improper characterizations of the claim language and Hinton. As Appellants had previously argued, the combination of registers 104, 106 does not teach a single page frame number field. As was previously stated in Appellants' arguments for Claim 12, the Appellants respectfully wonder how a register could possibly teach a field. Thus, contrary to what the Examiner alleges, Hinton, at col. 6, lines 37-63, does not disclose anything about a single field for storing odd page frame numbers and a single field for storing even page frame numbers. While Hinton, at col. 6, lines 37-63, may disclose a register, Hinton does not disclose anything about a "field." Therefore, for at least these reasons, the Examiner's argument does not show a teaching of each and every element recited in Claim 16. Consequently, Claim 16 should be allowed. The Appellants request reversal of the rejection of Claim 16.

D. Dependent Claim 17

In the Examiner's Answer, the Examiner stated the following:

> Appellant's arguments directed to the rejection of claim 17, reiterate the alleged deficiencies Appellant pointed out with respect to claims 12 and 15. Accordingly, these arguments are addressed at least in the manner that claims 12 and 15 have been addressed above.
>
> *See* Examiner's Answer at page 34.

Claim 17 recites "system of Claim 16 wherein said buffer comprises a translation lookaside buffer of reduced size." Contrary to what the Examiner alleges, the Appellants respectfully argued that Claim 12 contains patentable subject matter. Appellants believe that Claim 17 is in condition for allowance for the reasons Appellants had provided for Claim 12. Since the Examiner indicates that she wishes to address Claim 17 in the same manner as she did for Claims 12 and 15, the Appellants request the Board to consider Appellants' arguments for Claims 12 and 15. Based on Appellants' arguments for Claims 12 and 15, Claim 17 is in condition for allowance. Consequently, the Appellants request reversal of the rejection to Claim 17.

E. Independent Claim 18

In the Examiner's Answer, the Examiner stated the following:

> Appellant's arguments directed to the rejection of claim 18, for the most part, reiterate the alleged deficiencies Appellant pointed out with respect to claims 12 and 15. Accordingly, these arguments are addressed at least in the manner that claims 12 and 15 have been addressed above.
>
> Appellant specifically states "Hinton's physical register 104 is used to store odd numbered pages while Hinton's physical register 106 is used to store

> even numbered pages. Thus, Hinton does not disclose ""a translation lookaside buffer, said translation lookaside buffer using a bit of a virtual page number of a virtual address for reading and writing odd and even page frame numbers using a single page frame number field of said translation lookaside buffer; a first register for mapping an even page frame number to said single page frame number field; and a second register for mapping an odd page frame number to said single page frame number field;" as recited in Claim 18. Instead, Hinton utilizes two separate memory to store even and odd pages;" however, the Examiner would like to respectfully point to Appellant that Appellant's own claim 18 requires a register for odd numbered page frame numbers and a register for even numbered page frame numbers, which comprise two separate memories. Refer to response to [A. Independent claim 12] above.
>
> Appellant argues the Examiner has not shown a teaching of "a first register for mapping an even page frame number to said single page frame number field; and a second register for mapping an odd page frame number to said single page frame number field;" however, the Examiner has identified "a first register for mapping an even page frame number to said single page frame number field" as [Hinton discloses "A logical address (81) is separated into three parts. Bits 0 through 11 are an offset within an instruction page" and explains that "bit 12 selects which of the two entries in the TWB (62) are to be used for this address... registers (106) marked "0" are for even-numbered pages" (col. 6, lines 37-63; fig. 3 and related text)] and "a second register for mapping an odd page frame number to said single page frame number field" as ["Registers (104) marked "1" are for odd-numbered 4KB pages, addresses for which bit 12 is a one" (Column 6, lines 37-63; fig. 3 and related text)].
>
> *See* Examiner's Answer at pages 34-35.

Claim 18 recites "a system to provide virtual to physical memory address translation of a translation lookaside buffer comprising: a translation lookaside buffer, said translation lookaside buffer using a bit of a virtual page number of a virtual address for reading and writing odd and

even page frame numbers using a single page frame number field of said translation lookaside buffer; a first register for mapping an even page frame number to said single page frame number field; and a second register for mapping an odd page frame number to said single page frame number field." Contrary to what the Examiner alleges, the Appellants respectfully argued that Claim 12 contains patentable subject matter. Appellants believe that Claim 18 is in condition for allowance for the reasons Appellants had provided for Claim 12. Furthermore, the Appellants had previously pointed out the deficiencies with respect to the Examiner's arguments for Claim 12.

Again, the Examiner restates the same argument made in Claim 12 by referencing Hinton, at col. 6, lines 37-63, and at Figure 3, in an attempt to show a teaching of Claim 18. Therefore, the Appellants respond with the same argument previously presented for Claim 12. Consequently, the Appellants request the Board to consider Appellants' arguments for Claim 12. For the same reasons presented in Claim 12, the Appellants respectfully submit that Hinton does not teach a "translation lookaside buffer using a bit of a virtual page number of a virtual address for reading and writing odd and even page frame numbers using a single page frame number field of said translation lookaside buffer," as recited in Claim 18. Hinton does not disclose anything about "using a single page frame number field of [a] translation lookaside buffer." While Hinton, at col. 6, lines 37-63, may disclose using even and odd registers within a translation *write buffer* (as specified in Hinton, at Figure 3), there is no disclosure within Hinton of "using a bit of a virtual page number of a virtual address for *reading and writing odd and even page frame numbers using a single page frame number field*," as recited in Claim 18. In particular, Hinton's *write buffer* does not teach *reading and writing* odd and even page frame numbers using a single page frame number field. Therefore, for at least these reasons, the

Examiner's argument does not show a teaching of each and every element recited in Claim 18. Consequently, Claim 18 should be allowed. The Appellants request reversal of the rejection of Claim 18.

F. Dependent Claim 19

In the Examiner's Answer, the Examiner states the following:

> Appellant's arguments directed to the rejection of claim 19, reiterate the alleged deficiencies Appellant pointed out with respect to claims 12 and 15. Accordingly, these arguments are addressed at least in the manner that claims 12 and 15 have been addressed above.

See Examiner's Answer at page 35.

Claim 19 recites "the system of Claim 18 wherein using a single page frame number field implements a reduced size of said translation lookaside buffer."

In response to the Examiner's remarks, the Appellants respectfully submit that Claim 19 contains patentable subject matter for the reasons presented by the Appellants in Claims 12 and 15, for example. Contrary to what the Examiner alleges, the Appellants respectfully argued that Claim 12 contains patentable subject matter, as the Appellants respectfully pointed out the deficiencies with respect to the Examiner's arguments. Appellants believe that Claim 19 is in condition for allowance for the reasons Appellants had provided for Claim 12. Therefore, for at least these reasons, Claim 19 is in condition for allowance. Since the Examiner wishes to address Claim 19 in the same manner as she did for Claims 12 and 15, the Appellants request the Board to consider Appellants' arguments for Claims 12 and 15.

G. Independent Claim 21

In the Examiner's Answer, the Examiner states the following:

Appellant's arguments directed to the rejection of claim 21, for the most part, reiterate the alleged deficiencies Appellant pointed out with respect to claims 12 and 15. Accordingly, these arguments are addressed at least in the manner that claims 12 and 15 have been addressed above.

Appellant argues Hinton does not disclose a "bit used to reduce size of said translation lookaside buffer by way of consolidating two page frame number fields of said indexed entry into said single page fame number field." In response, this argument has been fully considered, but it is not deemed persuasive since Hinton clearly discloses [when bit 12 is a 0, TWB (Translation Write Buffer or mini-TLB) will read and write in a single field within Physical Register 0 (which is used for even pages), which comprises reading and writing even page frame numbers into a single page frame number field of a translation lookaside buffer. For further explanation, when bit 12 is a 1, TWB will read and write into a single field within Physical Register 1 (which is used for odd pages), which comprises consolidating even and odd page frame numbers into a single page frame number field]. Note that registers 104 (odd pages) and 106 (even pages) used to store logical to physical address sets are interpreted as a single page frame number field for even and odd page frame numbers; even page frame numbers are only stored in register 106 and odd page frame numbers are only stored in register 104. Further note that a reduction in size is a generic property in Hinton's TWB wherein Hinton discloses ["Mini-TLB (TWB)," defined as "A small 3-entry instruction mini TLB (6)" (Columns 5-6, lines 62-67 and 1-5) which is of mini/reduced size]. Refer to Response to [A. Independent Claim 12 and B. Dependent Claim 15] above.

See Examiner's Answer at pages 35-36.

Claim 21 recites "a method comprising: obtaining a bit obtained from a virtual page number of a virtual address; using said bit to determine which one of two storage registers will be used for:

a) writing page frame number data from said one of two storage registers into an indexed entry of a single page frame number field of said translation lookaside buffer, said two storage registers comprising a first storage register used for writing even page frame numbers into said single page frame number field when said bit is a first value and a second storage register used for writing odd page frame numbers into said single page frame number field when said bit is a second value, or

b) reading said page frame number data from said single page frame number field, said first storage register used to read said page frame number data when said bit is said first value, said second storage register used to read said page frame number data when said bit is said second value, said bit used to reduce size of said translation lookaside buffer by way of consolidating two page frame number fields of said indexed entry into a single page frame number field."

Contrary to what the Examiner alleges, the Appellants respectfully argued that Claim 12 contains patentable subject matter. Appellants believe that Claim 21 is in condition for allowance for the reasons Appellants had provided for Claim 12. Furthermore, the Appellants had previously pointed out the deficiencies with respect to the Examiner's arguments for Claim 12. Therefore, for at least these reasons, Claim 21 is in condition for allowance.

The Appellants respectfully submit that Claim 21 should be allowed for at least the reasons pointed out by the Appellants in Claim 15. The Examiner has referenced Hinton, at cols. 5-6, lines 62-67 and 1-5. While Hinton, at cols. 5-6, lines 62-67 and 1-5, may disclose a buffer of reduced size, there is no disclosure in Hinton that discloses a method comprising "obtaining a bit obtained from a virtual page number of a virtual address; using said bit to determine which one of two storage registers will be used for writing page frame number data from said one of

two storage registers into an indexed entry of a single page frame number field of said translation lookaside buffer, said two storage registers comprising a first storage register used for writing even page frame numbers into said single page frame number field when said bit is a first value and a second storage register used for writing odd page frame numbers into said single page frame number field when said bit is a second value," as recited in Claim 21. Furthermore, there is no disclosure in Hinton that teaches a method comprising "obtaining a bit obtained from a virtual page number of a virtual address; using said bit to determine which one of two storage registers will be used for reading said page frame number data from said single page frame number field, said first storage register used to read said page frame number data when said bit is said first value, said second storage register used to read said page frame number data when said bit is said second value," as recited in Claim 21. Furthermore, there is no disclosure in Hinton of "said bit used to reduce size of said translation lookaside buffer by way of consolidating two page frame number fields of said indexed entry into a single page frame number field," as recited in Claim 21.

Furthermore, Hinton discloses pairs of registers employed *within* (inside) a translation write buffer (TWB) that are used for storing data within the TWB. In other words, Hinton's TWB comprises pairs of registers. This is different from what is recited in Claim 21. As illustratively described in Figures 3-6 of the present Application and as stated in paragraph 26 of the present Application, the mini-TLB communicates with a number of registers located outside of the TLB. Thus, Hinton does not teach "using said bit to determine which one of two storage registers will be used for *writing* page frame number data *from* said one of two storage registers *into* an indexed entry of a single page frame number field of said translation lookaside buffer, said two storage registers comprising a first storage register used for writing even page frame

numbers into said single page frame number field when said bit is a first value and a second storage register used for writing odd page frame numbers into said single page frame number field when said bit is a second value," for example. In particular, Hinton does not teach anything about "writing page frame number data *from* said one of two storage registers *into* an indexed entry of a single page frame number field of said translation lookaside buffer," as recited in Claim 21.

Likewise, Hinton does not teach "using said bit to determine which one of two storage registers will be used for *reading* said page frame number data *from* said single page frame number field, said first storage register used to read said page frame number data when said bit is said first value, said second storage register used to read said page frame number data when said bit is said second value," as recited in Claim 21.

In addition, Hinton does not teach "said bit used to reduce size of said translation lookaside buffer by way of consolidating two page frame number fields of said indexed entry into a single page frame number field," as recited in Claim 21. As was argued in Claim 12, the Appellants pointed out that Hinton does not teach anything about reducing the size of a buffer by way of consolidating even and odd page frame number fields into a single page frame number field. The Appellants respectfully submit that for the same reasoning presented in Claim 12, Hinton does not teach "said bit used to reduce size of said translation lookaside buffer by way of consolidating two page frame number fields of said indexed entry into a single page frame number field," as recited in Claim 21.

Thus, contrary to what the Examiner alleges, Hinton, at cols. 5-6, lines 62-67 and 1-5, does not disclose anything about "obtaining a bit obtained from a virtual page number of a virtual address; using said bit to determine which one of two storage registers will be used for:

a) writing page frame number data from said one of two storage registers into an indexed entry of a single page frame number field of said translation lookaside buffer, said two storage registers comprising a first storage register used for writing even page frame numbers into said single page frame number field when said bit is a first value and a second storage register used for writing odd page frame numbers into said single page frame number field when said bit is a second value, or b) reading said page frame number data from said single page frame number field, said first storage register used to read said page frame number data when said bit is said first value, said second storage register used to read said page frame number data when said bit is said second value, said bit used to reduce size of said translation lookaside buffer by way of consolidating two page frame number fields of said indexed entry into a single page frame number field." Therefore, for at least the foregoing reasons, Claim 21 contains patentable subject matter that should be passed to allowance. The Appellants request the Board to reverse the rejection to independent Claim 21.

H. Independent Claim 29

In the Examiner's Answer, the Examiner states the following:

> Appellant's arguments directed to the rejection of claim 29, reiterate the alleged deficiencies Appellant pointed out with respect to claims 12, 15 and 21. Accordingly, these arguments are addressed at least in the manner that claims 12, 15 and 21 have been addressed above.

See Examiner's Answer at pages 36-37.

Claim 29 recites "a method of performing a write operation using a translation lookaside buffer comprising: using a bit of a virtual page number, said virtual page number stored in a data register; assessing whether a value of said bit of a virtual page number is 0 or 1; writing a first

page frame number stored in a first register to a page frame number field of an indexed entry of said translation lookaside buffer if said value is 0; and writing a second page frame number stored in a second register to said page frame number field of said indexed entry of said translation lookaside buffer if said value is 1, said indexed entry comprising a single page frame number field used to reduce the size of said translation lookaside buffer."

In response to the Examiner's remarks, the Appellants respectfully submit that Claim 29 contains patentable subject matter for the reasons presented by the Appellants in Claims 12, 15, and 21, for example. Contrary to what the Examiner alleges, the Appellants respectfully argued that Claim 29 contains patentable subject matter, as the Appellants respectfully pointed out the deficiencies with respect to the Examiner's arguments. Appellants believe that Claim 29 is in condition for allowance for the reasons Appellants had provided for Claims 12, 15, and 21. Therefore, for at least these reasons, Claim 29 is in condition for allowance. Since the Examiner wishes to address Claim 29 in the same manner as she did for Claims 12, 15, and 21, Appellants request the Board to consider Appellants' arguments for Claims 12, 15, and 21.

I. Independent Claim 32

In the Examiner's Answer, the Examiner states the following:

> Appellant's arguments directed to the rejection of claim 32, reiterate the alleged deficiencies Appellant pointed out with respect to claims 12, 15 and 21. Accordingly, these arguments are addressed at least in the manner that claims 12, 15 and 21 have been addressed above.
> *See* Examiner's Answer at page 37.

Claim 32 recites "a method of performing a read operation using a translation lookaside buffer comprising: using a bit of a virtual page number, said virtual page number stored in virtual

page number field of said translation lookaside buffer; assessing whether a value of a bit of a virtual page number is 0 or 1; reading a page frame number stored in a page frame number field of an indexed entry of said translation lookaside buffer; storing said page frame number into a first register if said value is 0; and storing said page frame number into a second register if said value is 1, said indexed entry comprising a single page frame number field used to reduce the size of said translation lookaside buffer."

In response to the Examiner's remarks, the Appellants respectfully submit that Claim 32 contains patentable subject matter for the reasons presented by the Appellants in Claims 12, 15, and 21, for example. Contrary to what the Examiner alleges, the Appellants respectfully argued that Claim 32 contains patentable subject matter, as the Appellants respectfully pointed out the deficiencies with respect to the Examiner's arguments. Appellants believe that Claim 32 is in condition for allowance for the reasons Appellants had pointed out for Claims 12, 15, and 21. Therefore, for at least these reasons, Claim 32 is in condition for allowance. Since the Examiner wishes to address Claim 32 in the same manner as she did for Claims 12, 15, and 21, Appellants request the Board to consider Appellants' arguments for Claims 12, 15, and 21.

J. Independent Claim 34

In the Examiner's Answer, the Examiner states the following:

> Appellant's arguments directed to the rejection of claim 34, for the most part, reiterate the alleged deficiencies Appellant pointed out with respect to claims 12, 15 and 21. Accordingly, these arguments are addressed at least in the manner that claims 12, 15 and 21 have been addressed above.
>
> Appellant argues the Examiner does not show a teaching of "using a virtual page number stored in a first register", "comparing said virtual page

number to one or more values stored in one or more virtual page number fields of one or more corresponding entries in said translation lookaside buffer" and "generating an identifying number associated with an entry of said one or more entries if a virtual page frame number stores a value that is equal to said virtual page number, and storing said identifying number into a second register".

In response, these arguments have been fully considered, but are not deemed persuasive.

Hinton discloses "using a virtual page number stored in a first register" as ["a logical address (81) is separated into three parts... Bit 12 selects which of the two entries in the TWB are to be used for this address... Registers (106) marked "0" are for even-numbered 4KB pages, addresses for which bit 12 is a zero. Registers (104) marked "1" are for odd-numbered 4KB pages, addresses for which bit 12 is a one" (Column 6, lines 37-63); TLB comprises another register]; "Comparing said virtual page number to one or more values stored in one or more virtual page number fields of one or more corresponding entries in said translation lookaside buffer" [Hinton discloses "the logical registers in the TWB compare bits 13 to 31 of this logical address with their stored values" wherein a hit or a miss would be detected (col. 7, lines 24-47)] and "generating an identifying number associated with an entry of said one or more entries if a virtual page frame number stores a value that is equal to said virtual page number, and storing said identifying number into a second register" [the value stored in the register wherein a hit is detected is gated to physical address bus, wherein bit 12 would be 0 for even entries and 1 for odd entries and sent to cache, which also comprises a register; wherein it is also taught that when logical address bits 0-11 match, the TWB stores the logical address in one of its entries (col. 6, lines 37-63; col. 7, lines 24-47; figs. 3 and 7 and related text)].

See Examiner's Answer at pages 37-38.

Claim 34 recites "a method of probing for a particular virtual page number of an entry in a translation lookaside buffer comprising: using a virtual page number stored in a first register;

comparing said virtual page number to one or more values stored in one or more virtual page number fields of one or more corresponding entries in said translation lookaside buffer; generating an identifying number associated with an entry of said one or more entries if a virtual page number field stores a value that is equal to said virtual page number; and storing said identifying number into a second register."

In response to the Examiner's remarks, the Appellants respectfully submit that Claim 34 contains patentable subject matter for the reasons presented by the Appellants in Claims 12, 15, and 21, for example. Contrary to what the Examiner alleges, the Appellants respectfully argued that Claim 34 contains patentable subject matter, as the Appellants respectfully pointed out the deficiencies with respect to the Examiner's arguments. Appellants believe that Claim 34 is in condition for allowance for the reasons Appellants had provided for Claims 12, 15, and 21. Therefore, for at least these reasons, Claim 34 is in condition for allowance. Since the Examiner wishes to address Claim 34 in the same manner as she did for Claims 12, 15, and 21, Appellants request the Board to consider Appellants' arguments for Claims 12, 15, and 21.

Furthermore, the Examiner again cites Hinton, at col. 6, lines 37-63, and at col. 7, lines 24-47; figs. 3 and 7 in an attempt to show a teaching of Claim 34. However, Hinton, at col. 6, lines 37-63, and at col. 7, lines 24-47; figs. 3 and 7 does not teach the second, third, and fourth clauses of Claim 34. While Hinton discloses using pairs of registers to show the operation of a typical TWB, nowhere does Hinton disclose what is recited in the second, third, and fourth clauses of Claim 34. For example, Hinton does not disclose anything about "comparing said virtual page number to one or more values stored in one or more virtual page number fields of one or more corresponding entries in said translation lookaside buffer." For example, Hinton does not disclose anything about "virtual page number fields." In particular, for example, Hinton

does not disclose anything about an "identifying number associated with an entry of said one or more entries." Likewise, Hinton does not disclose anything about "generating an identifying number associated with an entry of said one or more entries if a virtual page number field stores a value that is equal to said virtual page number." Nor does Hinton disclose anything about "storing said identifying number into a second register." Nothing in Hinton, at col. 6, lines 37-63, and at col. 7, lines 24-47; figs. 3 and 7, teaches or discloses what is recited in the third or fourth clauses of Claim 34, for example. Therefore, the Examiner has not shown a teaching of each and every element recited in Claim 34. Consequently, Claim 34 should be allowed. Based on the foregoing, the Appellants request a reversal of the rejection of Claim 34.

K. Independent Claim 41

In the Examiner's Answer, the Examiner states the following:

> Appellant's arguments directed to the rejection of claim 41, reiterate the alleged deficiencies Appellant pointed out with respect to claims 12, 15 and 21. Accordingly, these arguments are addressed at least in the manner that claims 12, 15 and 21 have been addressed above.
>
> Appellant argues Hinton does not disclose "a page frame number field used to store an even or an odd page frame number, said even or said odd page frame number indicated by a bit from said virtual page number;" however, Examiner strongly disagrees as Hinton discloses a page frame number field used to store an even [register 106 (fig. 3 and related text; col. 6, lines 37-63)] OR (note that only ever OR odd is required by claim 41. which claims limitations in the alternative form) an odd [register 104 (fig. 3 and related text; col. 6, lines 37-63)] page frame number, said even or said odd page frame number indicated by a bit from said virtual page number [Hinton discloses bit 12, if zero, selects even page frame number (register 106) OR if 1, selects odd page frame number

(register 1047) (fig. 3 and related text; col. 6, lines 37-63)]. Further Refer to Response to [A. Independent Claim 12, B. Dependent Claim 15 and G. Independent Claim 21] above.

See Examiner's Answer at pages 38-39.

Claim 41 recites "a reduced size translation lookaside buffer comprising: a virtual page number field used to store a virtual page number; a page frame number field used to store an even or an odd page frame number, said even or said odd page frame number indicated by a bit from said virtual page number."

In response to the Examiner's remarks, the Appellants respectfully submit that Claim 41 contains patentable subject matter for the reasons presented by the Appellants in Claims 12, 15, and 21, for example. Contrary to what the Examiner alleges, the Appellants respectfully argued that Claim 41 contains patentable subject matter, as the Appellants respectfully pointed out the deficiencies with respect to the Examiner's arguments. Appellants believe that Claim 41 is in condition for allowance for at least the reasons provided in Appellants' response to Claim 12, for example. As was previously stated in Appellants' argument for Claim 12, a register does not teach a field. Therefore, for at least these reasons, Claim 41 is in condition for allowance. Since the Examiner wishes to address Claim 41 in the same manner as she did for Claims 12, 15, and 21, Appellants request the Board to consider Appellants' arguments for Claims 12, 15, and 21.

II. REJECTION OF CLAIM 24 UNDER 35 U.S.C. § 103(a) AS BEING UNPATENTABLE OVER HINTON

A. Dependent Claim 24

In the Examiner's Answer, the Examiner states the following:

In response to Appellant's remark that the Examiner does not provide

proper motivation to modify Hinton to incorporate a MIPS control processor instruction set as "Appellants do not see how selecting from off the shelf processors at least to reduce cost and take advantage of existing component design has anything to do with combining the teachings of Hinton with a MIPS control processor instruction set."

In response, this remark has been fully considered, but it is not deemed persuasive.

Sources of rationale supporting a rejection under 35 U.S.C. 103 may be in a reference, or reasoned from common knowledge in the art, scientific principles, art recognized equivalents, or legal precedent. The CCPA has held that "in considering the disclosure of a reference, it is proper to take into account not only specific teachings of the reference but also the inferences which one skilled in the art would reasonably be expected to draw therefrom."

In re Preda, 401 F.2d 825,826, 159 USPQ 342, 344 (CCPA 1968); MPEP 2144.01

In determining obviousness under 35 U.S.C. 103 in view of the Supreme Court decision in KSR International Co. v. Teleflex Inc., the Supreme Court stated that: "If a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill".

Still further, the Court states that "the focus when making a determination of obviousness should be on what a person of ordinary skill in the pertinent art would have known at the time of the invention...and this is regardless of whether the source of that knowledge and ability was documentary prior art, general knowledge in the art, or common sense".

The examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one

> of ordinary skill in the art. See In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).
>
> In this case, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to use an existing processor instruction set, such as MIPS (Millions Instructions Per Second) and make the translation lookaside buffer as taught by Hinton compatible with existing instructions, software, or commands as one of ordinary skill in the art would have been motivated to select from off the shelf processors at least to reduce cost and take advantage of existing components. Thus, the examiner has provided a motivation one of ordinary skill would have had to make an invention compatible with a MIPS (Millions Instructions Per Second) processor instruction set, which is a well-known processor type.
>
> In light of the forgoing, Examiner would like to accentuate that Hinton meets the claimed invention, as required by claim 24.
>
> *See* Examiner's Answer at pages 39-40.

Claim 24 recites "the method of Claim 23 wherein said TLB control processor instruction set comprises a MIPS control processor instruction set." As was previously questioned by the Appellants in the Appeal Brief, the Appellants stated that the Examiner had not provided a proper motivation to modify Hinton to incorporate "a MIPS control processor instruction set." The Examiner has restated the same motivation previously provided in the Office Action dated October 29, 2007, concerning the incorporation of "a MIPS control processor instruction set." As was previously questioned, the Appellants do not see how "select[ing] from off the shelf processors at least to reduce cost and take advantage of existing system component designs" has anything to do with a motivation for combining the teachings of Hinton with "a MIPS control processor instruction set," as recited in Claim 24. The Examiner has not provided a logical motivation. Consequently, the Appellants respectfully submit that the Examiner has not shown a

teaching of Claim 24. Thus, since a prima facie case of obviousness has not been established, Claim 24 should be passed to allowance. Furthermore, Claim 24 is allowable for at least the reason that Claim 24 depends on an allowable Claim 23. The Appellants request reversal of the rejection to Claim 24.

III. REJECTION OF CLAIMS 27 AND 28 UNDER 35 U.S.C. § 103(a) AS BEING UNPATENTABLE OVER HINTON IN VIEW OF REIDLINGER

A. Dependent Claim 27

In the Examiner's Answer, the Examiner states the following:

> Appellant argues "Appellants respectfully disagree that it would have been obvious for one of ordinary skill in the art to "use a page mask of any size, including a page mask that ranges from 4 kilobytes to 16 megabytes or that comprises 4 kilobytes for virtual to physical address mapping, such as the system taught by Hinton." Furthermore, Appellants respectfully disagree that it would have been obvious to utilize a page mask size ranging from 4 kilobytes to 16 megabytes, as recited in Claim 27," that the Examiner has not produced a prima facie case, thus "the Appellant is under no obligation to submit evidence of unobviousness", and that "the Examiner has not provided any suggestion or motivation, to support this conclusion."
>
> These arguments have been fully considered, but are not deemed persuasive.
>
> First, the Examiner refutes Appellant's argument that the Examiner has not provided a prima facie, as evidence, [sic] refer to Final Office Action mailed on 10/29/2007.
>
> The Examiner deems that it would have been obvious to one of ordinary skill in the art to [use a page mask of any size, including a page mask that ranges from 4 kilobytes to 16 megabytes or that comprises 4 kilobytes for virtual to physical address mapping] as the size of a page mask is a matter of design choice

as it appears that the invention would perform equally well with any size of page mask. The reference to Riedlinger has been provided as proof that it is well known in the art at time of the invention that the page mask size is used to selected [sic] a virtual page size.

Note that the page mask size as used in the various aspects of Appellant's claimed invention provides a preferred embodiment (i.e., a preferred range) in which the claimed invention may be realized; wherein it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Furthermore, the recitations of "wherein said virtual address utilizes a page mask size ranging from 4 kilobytes to 16 megabytes" or "wherein said page mask size comprises 4 kilobytes;" is a mere change in size of a virtual page mask size. A change is size is generally recognized as being within the level of ordinary skill in the art. In re Rose, 105 USPQ 237 (CCPA 1955).

Further, refer to response of [II. A. Dependent Claim 24] above wherein it is shown that sources of rationale supporting a rejection under 35 U.S.C. 103 may be in a reference, or reasoned from common knowledge in the art, scientific principles, art recognized equivalents, or legal precedent.

See Examiner's Answer at pages 41-43.

Claim 27 recites "the method of Claim 25 wherein said virtual address utilizes a page mask size ranging from 4 kilobytes to 16 megabytes." While the Examiner believes that "it would have been obvious to one of ordinary skill in the art to use a page mask of any size," and has provided a reference (Riedlinger) in an attempt to show a teaching of "a page mask size ranging from 4 kilobytes to 16 megabytes," the Examiner has not provided a motivation to combine Hinton and Riedlinger in this 103 (a) rejection. Furthermore, the Examiner has not indicated where within Riedlinger there is a teaching of "a page mask size ranging from 4

kilobytes to 16 megabytes." Consequently, the Examiner has not established a prima facie case of obviousness. Therefore, the Appellants request the Board to reverse the rejection to Claim 27.

B. Dependent Claim 28

In the Examiner's Answer, the Examiner states the following:

> Appellant's arguments directed to the rejection of claim 28, reiterate the alleged deficiencies Appellant pointed out with respect to claim 27. Accordingly, these arguments are addressed at least in the manner that claim 27 has been addressed above.

See Examiner's Answer at page 44.

Claim 28 recites "the method of Claim 27 wherein said page mask size comprises 4 kilobytes." Since the Examiner indicates that she is addressing Claim 28 in the same manner addressed for Claim 27, the Appellants respectfully submit that Claim 28 should be allowed for the same reasons Appellants had presented for Claim 27.

IV. REJECTION OF CLAIMS 35-38 AND 40 UNDER 35 U.S.C. § 103(a) AS BEING UNPATENTABLE OVER APPLICANT ADMITTED PRIOR ART (AAPA) IN VIEW OF HINTON

A. Independent Claim 35

In the Examiner's Answer, the Examiner states the following:

> Appellant's arguments directed to the rejection of claim 35, reiterate the alleged deficiencies Appellant pointed out with respect to claims 12, 15 and 21. Accordingly, these arguments are addressed at least in the manner that claims 12, 15 and 21 have been addressed above. Refer to rejection to claim 35 in Grounds of Rejection above.

See Examiner's Answer at page 44.

Claim 35 recites "A translation lookaside buffer system comprising: a translation lookaside buffer; a first register used for storing a value that indexes an entry in said translation lookaside buffer, said entry comprising a virtual page number field and a single page frame number field; a second register used for storing a page size of said entry; a third register used for storing a virtual page number of said entry, said virtual page number comprising a bit; a fourth register used for storing an even page frame number; and a fifth register used for storing an odd page frame number, said bit of said virtual page number used to determine whether said even page frame number or said odd page frame number is to be stored in said page frame number field in said translation lookaside buffer when performing a write operation, said bit of said virtual page number stored in said virtual page number field used to determine whether said even page frame number is to be stored in said fourth register or said odd page frame number is to be stored in said fifth register when performing a read operation, wherein use of said single page frame number field reduces the size of said translation lookaside buffer."

The Appellants respectfully submit that the Examiner has not shown a teaching of each and every element recited in independent Claim 35. The Examiner simply states that Claim 35 is rejected based on the Examiner's arguments for Claims 12, 15, and 21.

Contrary to what the Examiner alleges, the Appellants respectfully argued that Claims 12, 15, and 21 contain patentable subject matter. Appellants believe that Claim 35 is in condition for allowance for at least the reasons pointed out by the Appellants with respect to Claims 12, 15, and 21. Furthermore, the Appellants believe that Claim 35 is in condition for allowance because the Appellants had pointed out the deficiencies with respect to the Examiner's arguments for Claims 12, 15, and 21. Since the Examiner indicates that she wishes to address Claim 16 in the same manner as she did for Claims 12, 15, and 21 the Appellants request the Board to consider

Appellants' arguments for Claims 12, 15, and 21. Furthermore, Appellants maintain the arguments presented in the Appeal Brief.

B. Dependent Claim 37

In the Examiner's Answer, the Examiner states the following:

> Appellant's arguments directed to the rejection of claim 37, reiterate the alleged deficiencies Appellant pointed out with respect to claim 24. Accordingly, these arguments are addressed at least in the manner that claim 24 has been addressed above.

See Examiner's Answer at page 44.

Claim 37 recites "the method of Claim 36 wherein said TLB control processor instruction set comprises a MIPS control processor instruction set." Since the Examiner indicates that she is addressing Claim 37 in the same manner addressed for Claim 24, the Appellants respectfully submit that Claim 37 should be allowed for the same reasons Appellants' had presented for Claim 24.

CONCLUSION

Based on the foregoing arguments, the Appellants believe that the pending claims should be allowed. Consequently, the Appellants request the Board to reverse the rejections of the pending claims.

The Commissioner is hereby authorized to charge additional fee(s) or credit overpayment(s) to the deposit account of McAndrews, Held & Malloy, Account No. 13-0017.

Dated: December 15, 2008

Respectfully submitted,

/Roy B. Rhee/

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